Yixuan Zhuang

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Education

Fudan University Shanghai, China

College of Integrated Circuits and Micro-Nano Electronics

B.Eng. candidate in Microelectronics Science and Engineering, Shannon Program

Sep 2025 – expected 2029 · Cumulative GPA 3.89/4.0 · 60 credits

Conference Paper and Presentation

Yixuan Zhuang, Shiting Wang, Ruiyao Qin, and Keren Zhu. "Beyond Capacity Checks: Read-Trace Consistency in Systolic-Array Simulator Evaluation." *11th International Conference on Integrated Circuits and Microsystems* (ICICM 2026), Xi'an, China. Accepted.

Oral presentation, 17 October 2026. Best Presentation Award (session)

Research Experience

Accelerator dataflow simulation 2026

FDUROP Xiyuan Program · Faculty advisor Keren Zhu

- Led a three-student study of how SCALE-Sim accounts for memory traffic. We checked whether each read served by the simulator could be traced to a DRAM transfer that finished in time.
- Across 17 neural-network layer shapes, 333 of 459 buffer-constrained configurations failed the read check. All 153 large-buffer controls passed. Nine weight-stationary cases still failed even though the distinct input and weight addresses fit in their respective active buffer regions.

GPU memory-system co-simulation Apr 2026 – present

Undergraduate research project, Fudan University

- Contributed to a group project comparing a C++ GPU model with RTL. Submitted a pull request for an L2 cache observer to the Accel-Sim project's GPGPU-Sim repository.
- In a replay of one Rodinia backprop trace, the observer recorded 61,275 accepted L2 accesses. Counts matched the simulator's native statistics for every access status.

Selected Technical Project

Model2GDS — ISSCC 2027 Code-a-Chip Oct–Nov 2026

The IEEE SSCS Open-Source Ecosystem merged the notebook and supporting files into its official Code-a-Chip repository. Model predictions matched SystemVerilog RTL for both numerical results and cycle counts in all 441 test runs across 2×2, 4×4, and 8×8 systolic arrays for matrix multiplication. A separate 20 ns study examined routed 2×2/4×4 area–latency trade-offs.

Selected Honors

East China Regional Second Prize, National College Student Integrated Circuit Innovation and Entrepreneurship Competition, LoongArch track (2026). Worked on C benchmarks comparing the original and optimized hardware for trigonometric functions.

Third Prize, 17th National Undergraduate Mathematics Competition, Shanghai (Non-Math A), 2025.

Fudan University Freshman Scholarship (2025).

First Prize, 41st Chinese Physics Olympiad (Jiangsu Division), 2024.

Skills and Languages

Python, C/C++, Linux, Git. Research tools used include SCALE-Sim, GPGPU-Sim, Verilator, and OpenROAD.

English: TOEFL iBT 5.0/6 (100/120), August 2026.